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Fp Dnn An Automated Framework

To overcome this problem, we propose FP-DNN (Field Programmable DNN), an end-to-end framework that takes TensorFlow-described DNNs as input, and automatically generates the hardware implementations on FPGA boards with RTL-HLS hybrid templates. FP-DNN performs model inference of DNNs with our high-performance computation engine and

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FP-DNN: An Automated Framework for Mapping Deep Neural Networks onto FPGAs with RTL-HLS Hybrid Templates. Abstract: DNNs (Deep Neural Networks) have demonstrated great success in numerous applications such as image classification, speech recognition, video analysis, etc. However, DNNs are much more computation-intensive and memory-intensive than previous shallow models.

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FP-DNN: An Automated Framework for Mapping Deep Neural Networks onto FPGAs with RTL-HLS Hybrid Templates. DNNs (Deep Neural Networks) have demonstrated great success in numerous applications such as image classification, speech recognition, video analysis, etc. [...] To overcome this problem, we propose FP-DNN (Field Programmable DNN), an end-to-end framework that takes TensorFlow-described DNNs as input, and

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automatically generates the hardware implementations on FPGA boards with RTL-HLS ...

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Download Fp Dnn An Automated Framework For Mapping Deep Neural fp dnn an automated framework part. FP-DNN automatically generates the hardware im-plementation with RTL-HLS hybrid templates. Our framework can support almost all types of DNNs, and we implement several DNNs (CNNs, LSTM-RNNs, and Residual Nets) as case studies. FPGA-based accelerators

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Yijin Guan et al. FP-DNN: An automated framework for mapping deep neural networks onto FPGAs with RTL-HLS hybrid templates. In Proc. of FCCM, 2017. Google Scholar; Yufei Ma et al. An automatic RTL compiler for high-throughput FPGA implementation of diverse deep convolutional neural networks. In Prof. of FPL, 2017. Google Scholar

Cloud-DNN: An Open Framework for Mapping DNN Models to ...

To enable fast and effective DNN chip design, we propose AutoDNNchip - a DNN chip generator that can automatically produce both FPGA- and ASIC-based DNN chip implementation (i.e., synthesizable RTL code with optimized algorithm-to-hardware mapping) from DNNs developed by machine learning

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frameworks (e.g., PyTorch) for a designated application and dataset without humans in the loop.

AutoDNNchip: An Automated DNN Chip Predictor and Builder ...

HybridDNN provides an end-to-end design framework which can generate high-performance instruction-based DNN accelerator designs and FPGA implementations in four steps (Figure 1). In Step (1), the targeted FPGA specification and the pretrained DNN model are passed to HybridDNN parser to capture hardware resource availability and DNN structure.

HybridDNN: A Framework for High-Performance Hybrid DNN ...

02/10/20 - Deep Neural Networks (DNN) represent a performance-hungry application. Floating-Point (FP) and custom floating-point-like arithmetic

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A Framework for Semi-Automatic Precision and Accuracy

...

FP-DNN: An Automated Framework for Mapping Deep Neural Networks onto FPGAs with RTL-HLS Hybrid Templates. (Peking University, HKUST, MSRA, UCLA) Compute-intensive part: RTL-based generalized matrix multiplication kernel. Layer-specific part: HLS-based control logic. Memory-intensive part: Several techniques for lower DRAM bandwidth requirements.

GitHub - fengbintu/Neural-Networks-on-Silicon: This is a

...

To overcome this problem, we propose FP-DNN (Field Programmable DNN), an end-to-end framework that takes TensorFlow-described DNNs as input, and automatically generates the hardware implementations on FPGA boards with RTL-HLS hybrid templates.

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By covering such diverse topics as DNN-to-accelerator toolflows, high-throughput cascaded classifiers and domain-specific model design, the presented set of works aim to enable the deployment of...

(PDF) Deploying Deep Neural Networks in the Embedded Space

Yijin Guan et al. [11] proposed a framework called FP-DNN, which automatically generates CNN accelerators based on RTL-HLS hybrid templates. In [12], an RTL-level CNN generator is proposed, whose input is a descriptive script from a previously trained CNN model. An HLS-based framework called fpgaConvNet is presented in [13].

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