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CS 331 Spring 2016

Notes on x86-64

Assembly Language

Our compilers will translate BPL code into Intel x86 assembly code.

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on x86-64 Assembly
Language Our
compilers will translate
BPL code into Intel x86
assembly code. Our lab
machines all use 64-bit
implementations of
Linux, so we will use
the 64-bit variant of
x86 code, which some

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denote by x86-64, or even by x64. To some extent ...

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Note that the %-e names were the names of the 32-bit registers in the old x86-32 architecture. Register Lower half Purpose
%rax %eax This is general purpose, but many people treat it as an “accumulator”,

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where the results of calculations go. The Intel programming conventions call for return values to be placed

x86-64 Assembler - Oberlin College Computer Science

X86-64 Assembly
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X86-64 Nomenclature
Due to the long history
of the x86 architecture,

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the terminology for data lengths can be somewhat confusing:
byte b 8 bits, no surprises there
short s 16-bit integer or 32-bit float
word w 16-bit value long l 32-bit integer or 64-bit float (aka double word)

Credits and Disclaimers X86-64 Assembly 1 - Computer Science

Access study documents, get

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answers to your study questions, and connect with real tutors for CS 331 : Algorithms and Complexity at University Of Texas.

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McQuain Preparing
Parameters The first 6
parameters are passed
in registers,
parameters 7 and up

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are passed on the stack. While there's are only 2 parameters in this example, note order of (unneeded) parameters on the stack: // caller int x, y;. . . int retval = max(x, y);. . . rbp old ...

Credits and Disclaimers X86-64 Calls 1 - Computer Science

CS 331: Data
Structures and
Algorithms

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Announcements. The Zoom meeting ID for our online lectures is 950 1330 6494 -- you can join using this link. We will be using Discord to run office hours, and it will also serve as our peer support and Q/A forum. If you aren't already a member, please join at <https://discord.gg/Kpxqbbp>. Calendar

CS 331: Data Structures and
Page 11/25

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Algorithms

CS:0 will point to the code segment and SS:0 to the stack segment. SP will be loaded with the size of the stack specified by the programmer, which is perfect because on the x86 a PUSH instruction decrements the stack pointer and then moves the pushed value into the memory addressed by SS:SP.

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Programming - Computer Science

MASM uses the standard Intel syntax for writing x86 assembly code. The full x86 instruction set is large and complex (Intel's x86 instruction set manuals comprise over 2900 pages), and we do not cover it all in this guide. For example, there is a 16-bit subset of the x86 instruction set.

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64 Assembly
Using the 16-bit
programming model
can be quite complex.

Guide to x86 Assembly - Computer Science

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cs-dept@alaska.edu

CS Home

Summary of GDB
commands for x86-64
Systems Command

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Effect Starting: gdb
gdb <file> Running
and stopping quit Exit
gdb run Run program
run 1 2 3 Run program
with command-line
arguments 1 2 3 ...
Note: Ctrl-C does not
exit from gdb, but halts
the current gdb
command Breakpoints

Summary of GDB commands for x86-64 Systems

CS 331 - Algorithms
and Complexity (233

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Documents) CS 314 -
CS 314 (217
Documents) CS 302 -
Pipelines and
Tunneling (216
Documents)

CS 331H : **Algorithms and** **Complexity - UT**

CS 331 : Algorithms
and Complexity; CS
331E : Elements of
Software Engineering II
; Past courses. CS 331 :
Algorithms and
Complexity (Fall 2015,

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Spring 2016, Fall 2016,
Fall 2017, Spring 2018,
Fall 2018, Fall 2019,
Spring 2020) CS 373 :
Software Engineering
(Fall 2016, Spring
2016, Summer 2020)
CS 311 : Discrete Math
for Computer Science
(Fall ...

Fares Fraij -
Department of
Computer Science
Young CS 331 D&A of
Algo. NP-Completeness
* With the Cook

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Theorem, we have the following property :
Lemma : If L_1 and L_2 belong to NP, L_1 is NP-complete, and $L_1 \leq L_2$ then L_2 is NP-complete. i.e. $L_1, L_2 \in \text{NP}$ and for all other $L' \in \text{NP}$, $L' \leq L_1$ and $L_1 \leq L_2 \leq L'$ $L_2 \leq L'$
Young CS 331 D&A of Algo.

Chapter 7. NP-Completeness

because the class project will require you to have familiarity with

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those specific instructions. Lecture Notes by David Wagner 3 of 14. Intel (x86) machines have another special register, called the instruction pointer (IP), that points to the next machine instruction to execute. For most machine instructions, the machine

**David Wagner CS
161 Computer
Security Notes
Memory safety ...**

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64 Assembly
3+dug´ dqg 3(dv\´
3ureohpv 3(dv\´
sureohpv fdq eh
vroyhg e\ sro\qrpldo
wlph dojrulwkp
6hduflqj sureohp
vruwlqj 'lmnvwud¶v
dojrulwkp pdwul[

5 P and NP

CS 161: Computer
Security.

Announcements:

Project 1 is due Friday,
September 25, 11:59
PM PT. Homework 1 is
due Friday, September

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11th, 11:59 PM PT.

Instructor: Nicholas
Weaver Lecture: Tu/Th,
12:30pm-2:00pm PT.
Show/hide optional
readings. Skip to
current week

CS 161 | CS 161: Computer Security

Note The issue does
not happen when
migrating from x86 to
x86 or x64 to x64
platforms. Opening
COMEXP.MSC or
DCOMCNFG.EXE and

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navigating to

Component

Services\Computers\My
Computer will result in
the following on-screen
error: You do not have
permission to perform
the requested action.

USMT 4.0 migration from x86 to x64 results in corrupted

...

A bit about the context
switch Typical actions
of the context switch.

Save and restore

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64 Assembly
registers; Switch

memory map; Do
magic; This is a very
hardware-dependent
action!. Usually context
switches begin with a
call to the kernel
routine `context_switch`.
`context_switch` calls a
machine-dependent
macro `switch_to` which
is defined with three
arguments as
`switch_to(prev, next,
last)`.

A bit about the
Page 23/25

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context switch -

Computer Science

CS:APP 3.2.2. 4.4

Where Does It Live •

Match (1-Processor /

2-Memory / 3-Disk

Drive) where each ... -

Note: A group of

wires/signals is

referred to as a bus [-

Thus, we say that

memories have ... In

x86-64, instructions

generally specify what

size data to access

from memory and then

operate upon. CS:APP

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3.3.
Language

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